IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) CDMA receiver for receiving a CDMA signal, which is transmitted at [[the]] a chip clock rate from a transmitter via various signal paths of a physical transmission channel, in a multi-subscriber environment having:

(a) a receiving device for receiving the CDMA signal;

(b) a Rake receiving circuit having a number of parallel-connected delay devices for detection of [[the]] signal components of the CDMA signal which are transmitted via the various signal paths;

(c) a channel estimation circuit for estimating channel coefficients h of a transmission channel H by means of a predetermined reference data sequence which is contained in the received CDMA signal;

(d) a weighting coefficient calculation device for calculating weighting coefficients m for the various signal components of the CDMA signal as a function of the estimated channel coefficients h and of stored spreading and scrambling codes;

(e) a weighting circuit for weighting the signal components with the calculated weighting coefficients m; and having

(f) a combiner for combining the weighted signal components to form an estimated received data signal.

2. (Previously Presented) CDMA receiving according to Claim 1, wherein the weighting coefficient calculation device is connected to a memory device.

3. (Currently Amended) CDMA receiving according to Claim 1, wherein spreading codes C_{SP} of the subscriber and scrambling codes C_{SC} from the transmitter are stored in [[the]] a memory device.

4. (Previously Presented) CDMA receiver according to claim 1, wherein the combiner is an adder for adding the weighted signal components.

5. (Previously Presented) CDMA receiver according to claim 1, wherein the reference data sequence is processed by the channel estimation circuit at the chip clock rate T_C.

6. (Previously Presented) CDMA receiving according to claim 1, wherein the delay devices of the Rake receiving circuit delay the received CDMA signal by an associated time delay τ differing by precisely one chip clock cycle T_C between the various delay devices.

7. (Canceled)

8. (Previously Presented) CDMA receiver according to claim 1, wherein an output circuit is provided for outputting the reference data sequence from the received CDMA received signal.

9. (Previously Presented) CDMA receiver according to claim 1, wherein the weighting circuit comprises a large number of multiplication circuits, which are each followed by a delay device.

10. (Canceled)

11. (Previously Presented) CDMA receiver according to claim 1, wherein the channel estimation circuit is a DSP processor.

12. (Previously Presented) CDMA receiver according to claim 1, wherein the weighting coefficient calculation device is a DSP processor.

13. (Previously Presented) CDMA receiver according to claim 2, wherein the memory device is an RAM memory.